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10/672,186	09/26/2003	Michael Thomas Greene	51249/RAG/Z74	9829

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EXAMINER	
MURRAY, DANIEL C	
ART UNIT	PAPER NUMBER
2443	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,186	GREENE, MICHAEL THOMAS	
	Examiner	Art Unit	
	DANIEL C. MURRAY	2443	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 OCT 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) *2,5 and 6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is in response to Applicant's amendment filed on 23OCT2009. **Claims 1-6** are now pending in the present application. **This Action is made FINAL.**

2. **Claims 2, 5, and 6** have been withdrawn from consideration by Applicant.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 1-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Andreev et al. (US Patent Publication # US 2001/0018759 A1)** in view of **Rostoker et al. (US Patent # 5,742,510).**

a) Consider **claim 1,** Andreev et al. clearly show and disclose, a computer implemented method of determining the routing (figure 2, abstract, paragraph [0002], paragraph [0088], paragraph

[0091], paragraph [0096]) of interconnected regions of a routing problem (figure 11a, figure 11b, figure 11c, figure 11d, abstract, paragraph [0148]), the interconnected regions being regions of an electrical circuit (figure 1, paragraph [0015], paragraph [0033], paragraph [0034]), the method comprising: routing all connections independently and in parallel (figure 2, figure 3, abstract, paragraph [0033], paragraph [0034], paragraph [0088], paragraph [0091], paragraph [0096]); assembling at least some contextual information about a region and the routing paths which cross in said region in the form of at least one conflict object (figure 2, figure 3, figure 8h, figure 9, abstract, paragraph [0089], paragraph [0102], paragraph [0124], paragraph [0143], paragraph [0187], paragraph [0210], paragraph [214]); and only resolving crossing conflicts only (figure 2, abstract, paragraph [0088], paragraph [0092], paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0190], paragraph [0211], paragraph [0215], paragraph [0277]) when said at least some contextual information has been assembled (figure 2, figure 3, figure 8h, figure 9, abstract, paragraph [0089], paragraph [0102], paragraph [0124], paragraph [0143], paragraph [0187], paragraph [0210], paragraph [214]). However, Andreev et al. does not specifically disclose routing all connections independently and in parallel (in the sense of being fully simultaneous) or each connection is routed while ignoring all other connections

Rostoker et al. show and disclose microelectronic circuit fabrication, and more specifically to an integrated circuit physical design automation system utilizing optimization process decomposition and parallel processing, wherein Rostoker et al. disclose considering all required connections independently and in parallel (figure 6, abstract, column 13 lines 52-36, column 21 lines 27-38), wherein each connection is routed while ignoring all other connections (abstract, column 14 lines 13-27, column 21 lines 27-38).

One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Rostoker et al. and Andreev et al. since both concern the art of microelectronic integrated circuit design and the automation of processes thereof and as such, both are with in the same environment.

Therefore, it would have been obvious to one of ordinary skill in the art that the time the invention was made to incorporate considering all required connections in parallel independently, as taught by, Rostoker et al. into the system of Andreev et al. for the purpose of optimized placement (cell/route)(Rostoker; abstract), thereby allowing the placement or cells/ routes to have the highest fitness.

b) Consider **claim 3,** and **as applied to claim 1 above,** Andreev et al. as modified by Rostoker et al. clearly show and disclose, the method according to claim 1, comprising the steps of:

(a) defining, for each set of regions to be connected (figure 11a, figure 11b, figure 11c, figure 11d, abstract, paragraph [0148]), routing which represents a suitable manner of connecting them (figure2, abstract, paragraph [0002], paragraph [0088], paragraph [0091], paragraph [0096], paragraph [0190]), respecting only those crossing conflicts (paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0211], paragraph [0215], paragraph [0277]) which have been explicitly registered with the set currently being considered (figure2, abstract, paragraph [0088], paragraph [0089]paragraph [0190]);

(b) examining connections across shared boundaries (paragraph [0148]);

(c) collating all such proposed routing and resolving any crossing conflicts (paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0211], paragraph [0215], paragraph

[0277]) in a symmetric manner (figure 2, abstract, paragraph [0033], paragraph [0089], paragraph [0091], paragraph [0096]);

(d) registering such crossing conflicts (paragraph [0145], paragraph [0146], paragraph [0187], paragraph [0188], paragraph [0211], paragraph [0215], paragraph [0277]) with the sets of regions which will be required to respect them on the next pass (figure 2, abstract, paragraph [0033], paragraph [0088]);

(e) repeating steps (a) to (c) until a sufficient completion and quality of routing solution is attained (paragraph [0092]); and

(f) converting the routing into suitable geometric representations of routing paths in a way which takes all desired routing into account symmetrically and simultaneously (figure 2, figure 3, figure 9, figure 10, figure 11a, abstract, paragraph [0033], paragraph [0038], paragraph [0088], paragraph [0093], paragraph [0095], paragraph [0096]).

c) Consider **claim 4**, and **as applied to claim 3 above,** Andreev et al. as modified by Rostoker et al. clearly show and disclose, the method according to claim 3, in which the regions are polygons (figure 11a, figure 11b, figure 11c) and the shared boundaries are edges (figure 11a, figure 11b, figure 11c, figure 11d, paragraph [0148]).

Response to Arguments

6. Applicant's arguments filed 23OCT2009 have been fully considered but they are not persuasive.

Applicant argues that "Andreev does not consider all connections in parallel independently; Andreev only considers all connections substantially in parallel independently (or simultaneously), or in parallel independently (or simultaneously) where they do not overlap. Indeed, Andreev's abstract (which is relied upon by Examiner) states, "A method for ... routing nets ... with parallel processors operating substantially simultaneously." Applicant is frankly surprised and disappointed that the Examiner continues to assert that Andreev shows a method that considers all connections in parallel independently, when it seemed during the telephone interview of September 19, 2008 that this distinction had been fully understood." and "routing all connections independently and in parallel, wherein each connection is routed while ignoring all other connections".

In response to Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Andreev clearly discloses considering a routing problem substantially simultaneously in parallel (figure 2, abstract, paragraphs [0088], [0096]). Andreev clearly discloses routing nets in an integrated circuit design, said method comprising the steps of dividing the integrated circuit design with lines in a first direction and lines in a second direction, forming a routing graph having vertices and edges, wherein vertices correspond to locations where lines in the first direction cross lines in the second direction, routing nets as a function of said routing graph with parallel processors

operating substantially simultaneously, determining the relative wire congestion among different areas in the integrated circuit design, and rerouting nets passing though areas with a relatively high wire congestion. Andreev clearly discloses the routing occurs independently and in parallel. The routing of Andreev consider the routes individually (independently), at the same time (in parallel).

However, what Applicant is arguing is that Andreev does not consider all routes simultaneously. During the interview (19SEP2008) Applicant is referring to Applicant stated that independently and in parallel necessarily meant simultaneously. Although the Examiner did not agree (discussed in further detail below), it was clear that in the case of overlap Andreev was substantially simultaneous and in the interests of furthering prosecution the Examiner introduced the Rostoker reference which clearly discloses a system in which cell placement/routing is considered simultaneously, independently and in parallel (abstract, column 21 lines 27-38) in order to find the optimized placement/routing.

Rostoker clearly discloses a placement optimization methodology is decomposed into a plurality of cell placement optimization processes that are performed simultaneously by parallel processors on input data representing the chip. The results of the optimization processes are recomposed to produce an optimized cell placement. The fitness of the optimized cell placement is analyzed, and the parallel processors are controlled to selectively repeat performing the optimization processes for further optimizing the optimized cell placement if the fitness does not satisfy a predetermined criterion. The system can be applied to initial placement, routing, placement improvement and other problems. Rostoker clearly discloses decomposing a cell placement/routing problem and considering everything (cell placement, routes, etc.) independently, simultaneously, and in parallel, recomposing the individual optimizations to create an optimized cell placement/routing,

and then consider its overall fitness and re-evaluating as necessary until the desired fitness is achieved.

Further, Andreev clearly discloses routing all connections independently and in parallel (figure 2, figure 3, abstract, paragraph [0033], paragraph [0034], paragraph [0088], paragraph [0091], paragraph [0096]). Andreev clearly discloses that individual routes are considered independently (individually without regard to other routes) and in parallel (concurrently). When an overlap between regions occurs Andreev considers the routes with respect to one region and then the other, while still considered independently and in parallel they are not however considered simultaneously. Rostoker clearly discloses that connection is routed while ignoring all other connections (abstract, column 14 lines 13-27, column 21 lines 27-38). Rostoker clearly discloses decomposing cell placement/routing into a plurality of cell placement/routing optimization processes that are performed simultaneously by parallel processors and that results of the optimization processes are recomposed to produce an optimized cell placement/routing. Rostoker clearly discloses that the individual processes are considered in independently, simultaneously, and in parallel (i.e. ignoring all other connections) and then are recomposed into am optimized cell placement/routing then reevaluated as necessary.

Therefore, the combination of Andreev and Rostoker clearly disclose routing all connections independently and in parallel, wherein each connection is routed while ignoring all other connections.

Applicant argues that "…the arguments previously set forth in the response submitted November 11, 2007 in response to the Office action of September 21, 2007. That response clearly demonstrated that:

a) Andreev is not able to route every net simultaneously;

b) Andreev's algorithm cannot be made fully simultaneous by any modification obvious to someone skilled in the art; and

c) In contrast, the method of the present invention routes all nets fully independently, simultaneously, and in parallel."

The Examiner respectfully disagrees.

In response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the features upon which applicant relies (i.e., consideration/routing simultaneously) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, Applicants arguments seem to hinge on simultaneity. During the interview to which Applicant is referring (19SEP2008) the Examiner argued that the claims did not include the term simultaneous, Applicant argued that independently and parallel necessarily included simultaneous. At the time the Examiner was unable to convince Applicant that this was not the case, that independent and parallel did not necessarily mean it was also simultaneous, although the Examiner remained unconvinced that it did, in the interested of furthering prosecution the Examiner introduced the Rostoker reference. In which Rostoker not only discloses consideration of a placement/routing problem independently, simultaneously, and in parallel but also discloses a situation where it is possible to operated both in parallel and independently, though not simultaneously (Rostoker, column 21 lines 27-38).

The Examiner has presented a clear and unambiguous *prima facie* case of obviousness that the claims are rejected based on the combination of Andreev and Rostoker. Yet, Applicant continues to argue without regard to Rostoker in most cases and especially with regard to simultaneity, which as

the Examiner has stated is not even clearly indicated in the claims. The above arguments (a, b, and c) where clearly addressed in detail in the Office Action sent in response to Applicant's response submitted November 11, 2007 and therefore are only briefly discussed here. The features as recited in the claims are clearly disclosed by Andreev and Rostoker. Applicant argues Andreev is not able to route every net simultaneously. While Andreev is not able to route every net simultaneously (only substantially simultaneously), Rostoker clearly is able to as discussed in detail above and in the previous Office Action(s).

Applicant argues Andreev's algorithm cannot be made fully simultaneous by any modification obvious to someone skilled in the art. Andreev's algorithm clearly can be made fully simultaneous by any modification obvious to someone skilled in the art. Rostoker clearly discloses a system which is capable of routing fully simultaneously, that is not only in the same field of endeavor but also indicates that the system disclosed therein can be applied to routing (discussed in detail below). Therefore it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Rostoker, into the system of Andreev (i.e. modify Andreev with the teachings of Rostoker) in order to make it fully simultaneous. Applicant argues that [in contrast to Andreev] the method of the present invention routes all nets fully independently, simultaneously, and in parallel.

There are two issues with this. Firstly, Applicant's argument with respect to Andreev does not take into account the fact that the rejection of Applicant's claims is made based on a combination of references, both Andreev and Rostoker. Andreev clearly discloses routing nets in parallel and independently, however, as Applicant has indicated not fully simultaneously. Rostoker clearly discloses routing that is not only independent and parallel but also simultaneous. Therefore the combination of Andreev and Rostoker clearly discloses routing all nets fully independently, simultaneously, and in parallel. Secondly, Applicant's argument is based on the supposition that

parallel and independent is necessarily simultaneous. This is clearly not the case as the Examiner attempted to explain in the interview on 19SEP2008 and as indicated in Rostoker (column 21 lines 27-38). Therefore, parallel and independent does not include simultaneous by default and therefore is not clearly recited in the claims. Furthermore, even if it was full simultaneity as Applicant is arguing was recited in the claims it is clearly taught by Rostoker as previously discussed.

Applicant argues "that a worker skilled in the art who read Rostoker and Andreev would [not] combine these to create the method claimed in the present application."

The Examiner respectfully disagrees.

One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Rostoker and Andreev since both concern the art of microelectronic integrated circuit design and the automation of processes thereof and as such, both are with in the same environment. Furthermore, Rostoker clearly discloses that the system can be applied to optimization problems in a number of diverse areas and specifically discloses that the system can be applied to routing (Rostoker; abstract, column 13 lines 47-64). Therefore, it would have been obvious to one of ordinary skill in the art that the time the invention was made to incorporate routing all required connections in parallel independently, as taught by, Rostoker into the system of Andreev because not only are they in the same field of endeavor but Rostoker also clearly discloses that the system disclosed by Rostoker can be applied not only to cell placement but also routing. In this case, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Rostoker and Andreev since both concern integrated circuit design and as such, both are with in the same environment (Andreev; paragraph [0002], Rostoker; column 1 lines 14-18), more particularly both clearly teach the routing of paths in

integrated circuits (Andreev; abstract, paragraph [0015] Rostoker; column 14 lines 13-27, column 16 lines 27-40).

Furthermore, the Examiner fails to see how it would not be obvious to combine Rostoker and Andreev when by Applicant's own admission "the Rostoker parallelisation would indeed be a sensible way to implement a parallelisation framework to support the separate routing tasks described in Andreev…" while Applicant goes on to argue that "...this would still not make Andreev able to route the nets fully in parallel, independently and simultaneously." the Examiner respectfully disagrees; Andreev clearly discloses the routing of interconnected regions independently, in parallel, and substantially simultaneously and Rostoker clearly discloses routing in parallel and simultaneously and since both Andreev and Rostoker concern integrated circuit design and as such, both are with in the same environment, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate independent, parallel, and simultaneous routing, as taught by, Rostoker into the system of Andreev for the purpose of allowing all connections to be considered simultaneously.

The majority, if not all, of Applicant's arguments have been addressed in previous Office Actions. It is requested that Applicant take the arguments presented in previous Office Actions as well as those present here into account when responding to this Office Action. Furthermore, while the Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the Applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Applicant, in preparing the responses, to fully consider each of the cited references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage

disclosed by the Examiner.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US 6,256,769 B1
- US 7,197,730 B1
- 4,831,725
- 6,011,912
- US 2002/0010901 A1
- US 2003/0084416 A1
- US 6,651,235 B2
- US 6,966,045 B2
- US 7,051,312 B1
- US 2007/0079264 A1
- US 7,065,729 B1
- US 6,378,121 B2
- US 6,330,707 B1
- 5,790,414
- 5,729,467
- 5,309,371

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL C. MURRAY whose telephone number is 571-270-1773. The examiner can normally be reached on Monday - Friday 0800-1700 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tonia Dollinger can be reached on (571)-272-4170. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. C. M./
Examiner, Art Unit 2443

/Tonia LM Dollinger/
Supervisory Patent Examiner, Art Unit 2443